

Gate Turn-Off Thyristor (GTO)

Integrated Gate Commutated Thyristor
•
(IGCT)

GTO

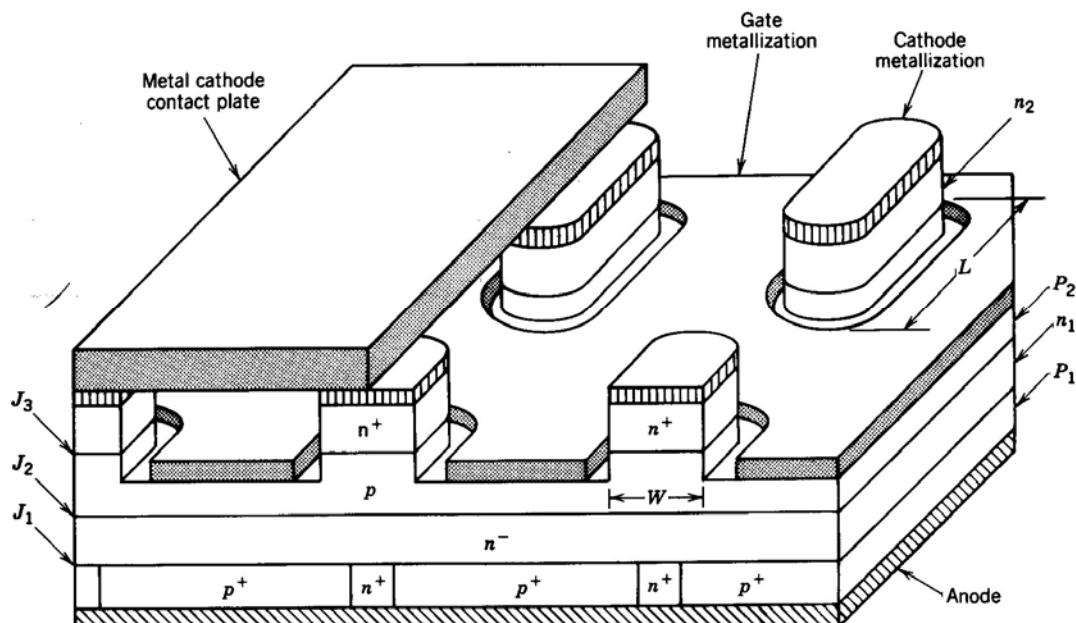


Figure 24-1 Vertical cross section and perspective view of a GTO.

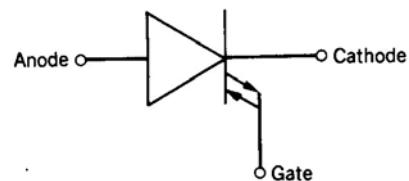
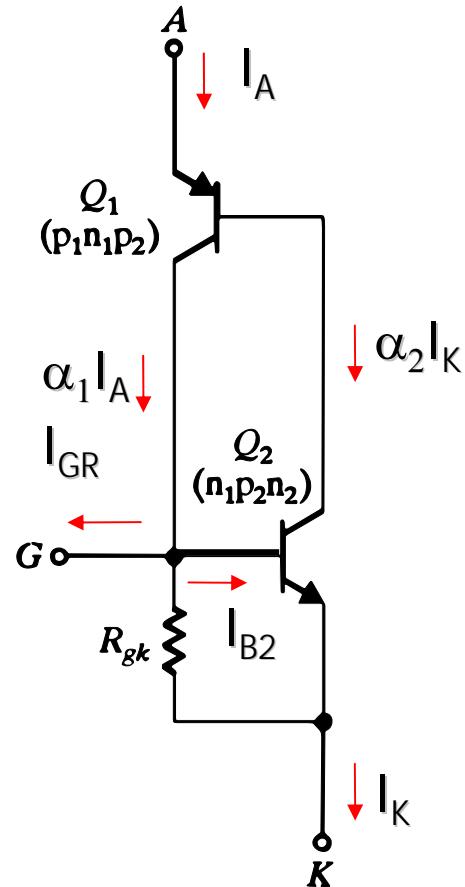


Figure 24-2 Circuit symbol for a GTO.

GTO



$$I_{B2} = \alpha_1 I_A - I_{GR} \quad (1)$$

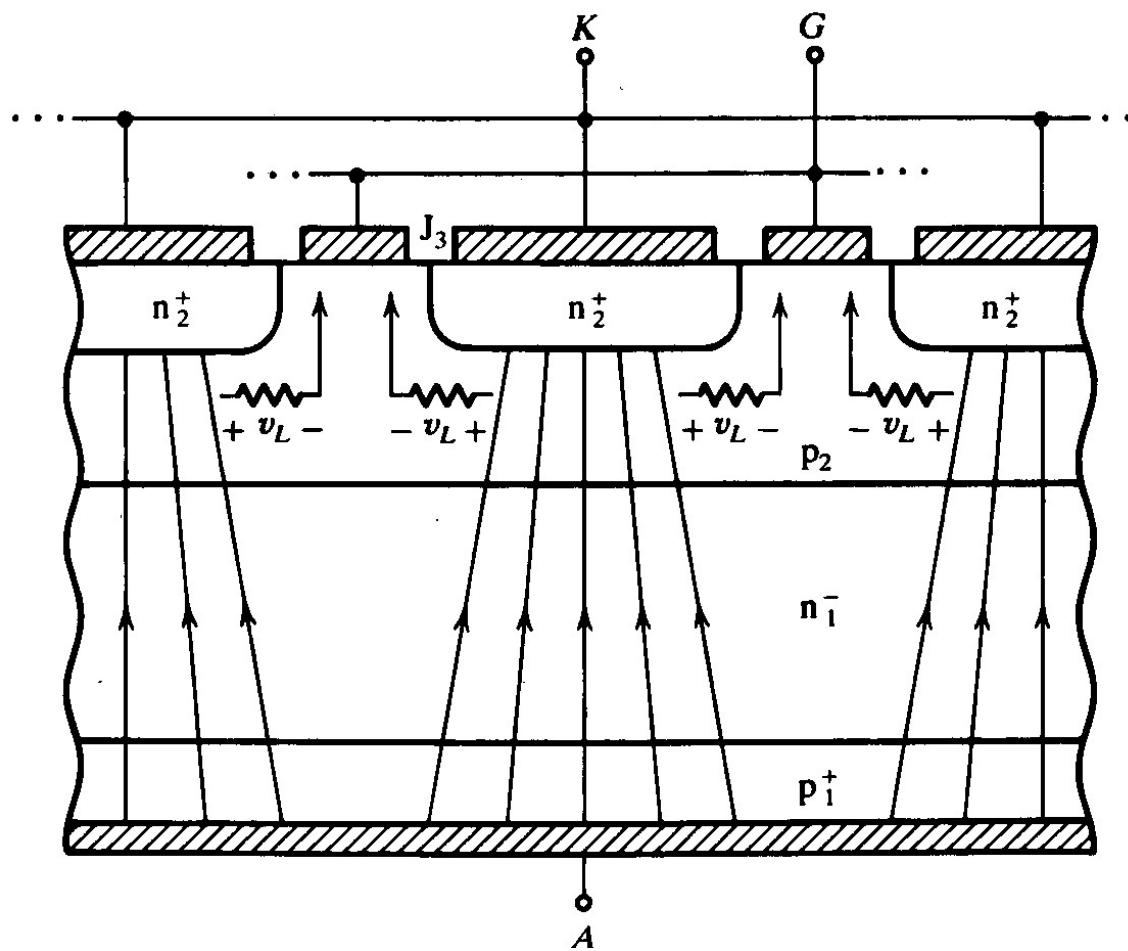
$$I_{B2} < (1 - \alpha_2) I_K \quad (2)$$

$$\alpha_1 I_A - I_{GR} < (1 - \alpha_2) I_K \quad : (2) \quad (1)$$

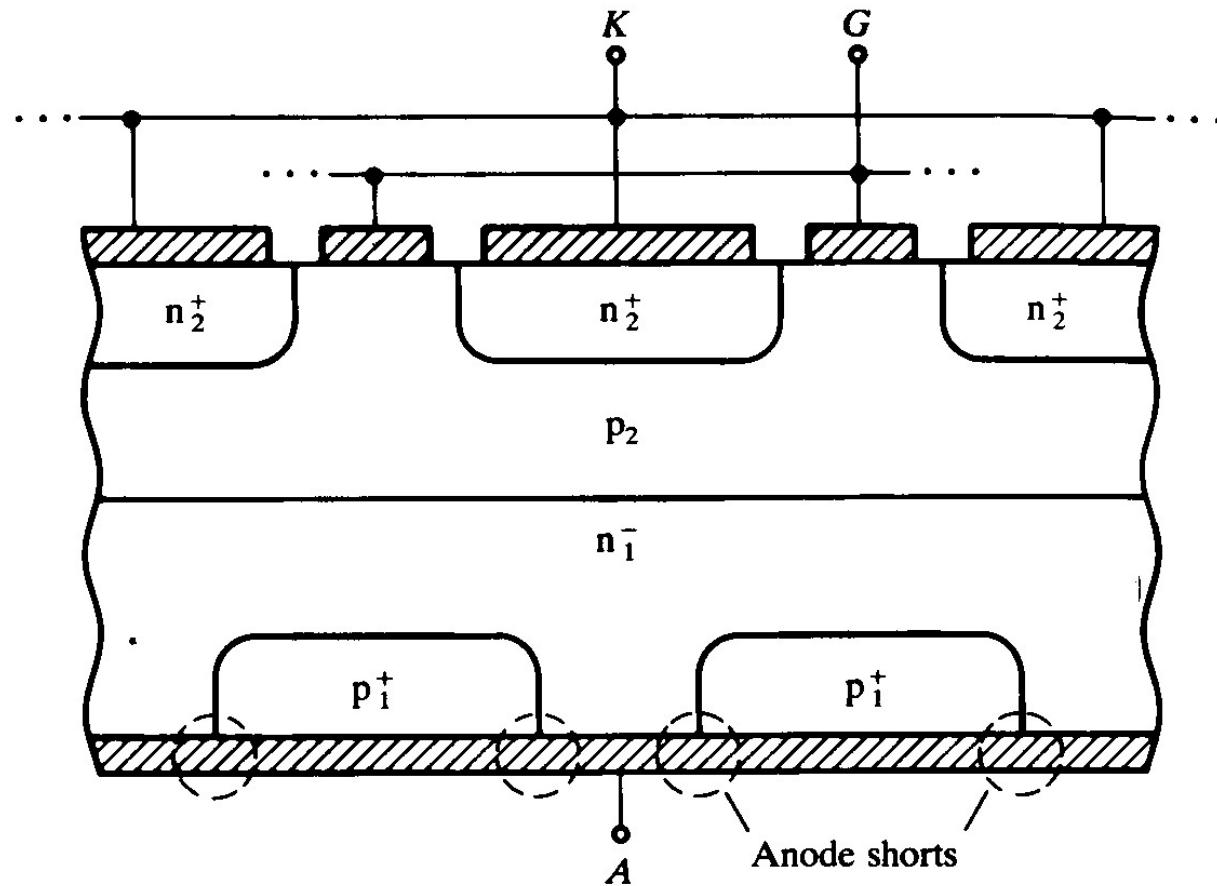
$$I_K = I_A - I_{GR} \quad (3)$$

$$I_{GR} / I_A > (\alpha_1 + \alpha_2 - 1) / \alpha_2 \quad (4)$$

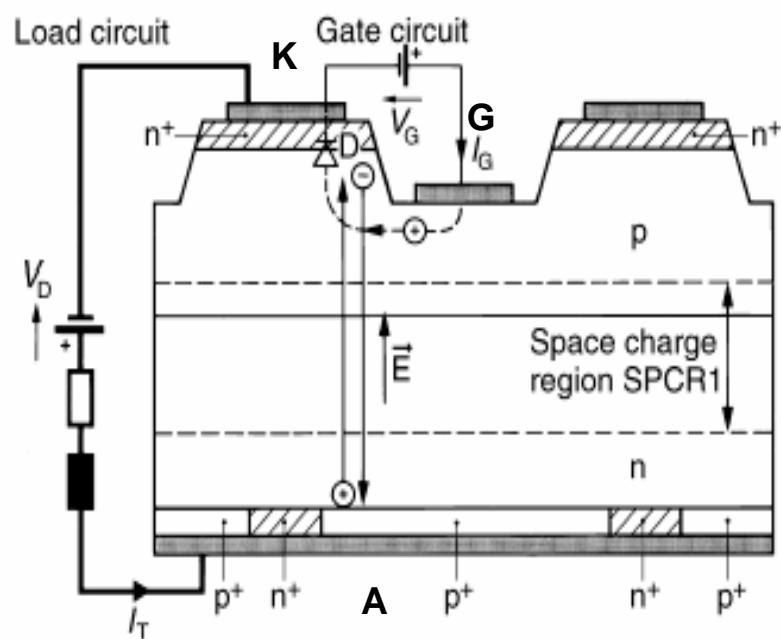
$$\beta = I_A / I_{GR} > \alpha_2 / (\alpha_1 + \alpha_2 - 1) \quad (5)$$



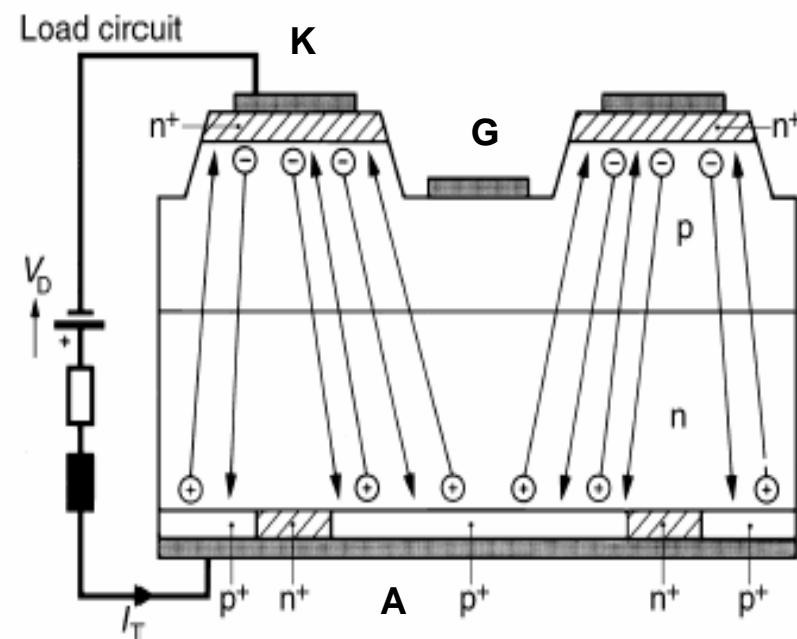
GTO



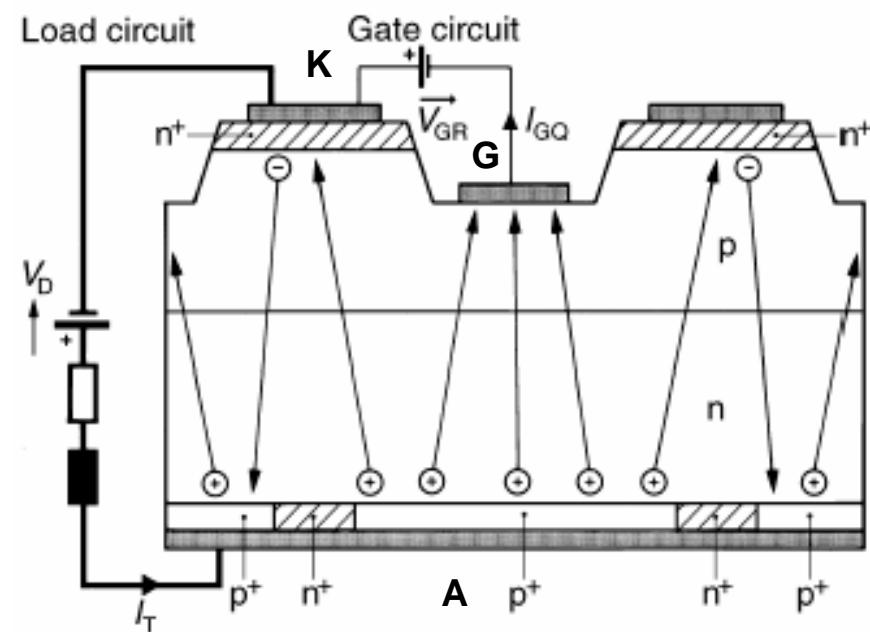
a) *Turn-On*



b) *On-State*



c) Turn-Off



d) Blocking State

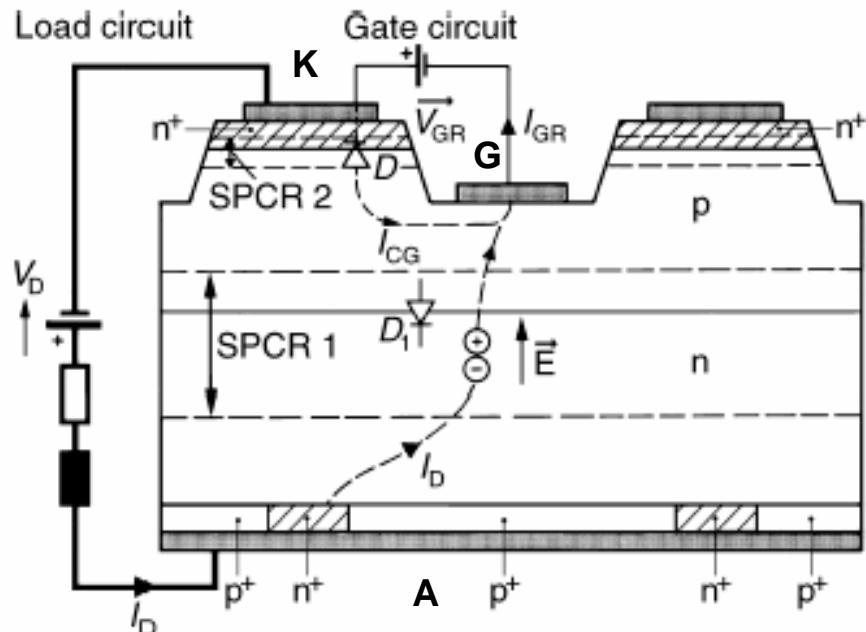


Fig. 2 Switching processes and operating states in the GTO: - electrons + holes

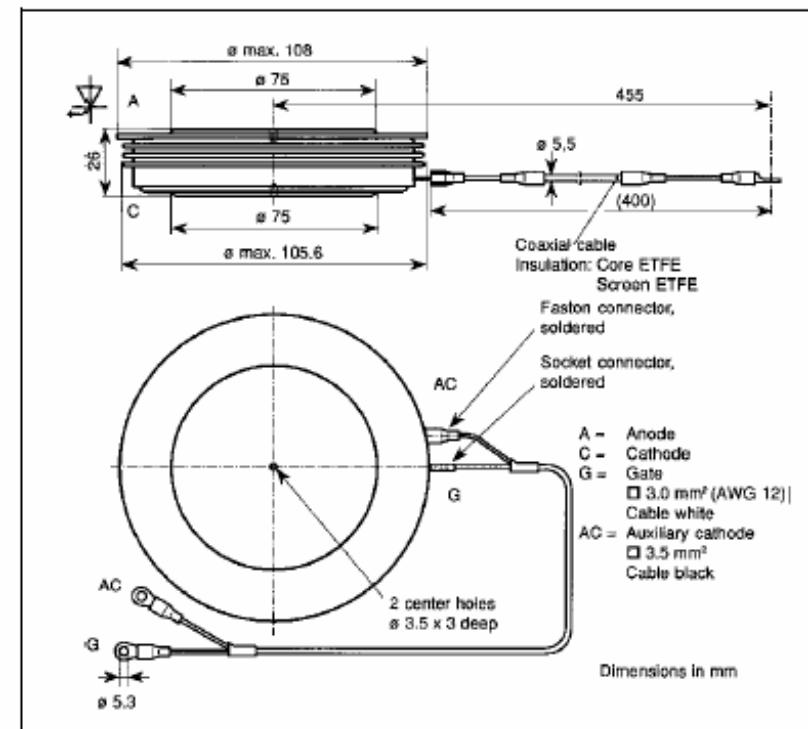
GTO

Gate turn-off Thyristor **5SGT 30J6004**

Doc. No. 5SYA 1212-04 April 98

Key Parameters

V_{DRM}	=	6000 V
I_{TGQM}	=	3000 A
I_{TSM}	=	24 kA
V_{TO}	=	1.70 V
r_T	=	0.60 mΩ
V_{DClink}	=	3800 V



Turn-on switching

di/dt_{crit}	Max. rate of rise of on-state current	400 A/ μ s	$f = 200Hz$	$I_T = 3000 A$	$T_j = 110 ^\circ C$
		800 A/ μ s	$f = 1Hz$	$I_{GM} = 25 A$	$di_G/dt = 25 A/\mu$ s
t_d	Delay time	2.5 μ s	$V_D = 0.5 V_{DRM}$	$T_j = 110 ^\circ C$	
t_r	Rise time	5.0 μ s		$I_T = 3000 A$	$di/dt = 300 A/\mu$ s
$t_{on(min)}$	Min. on-time	100 μ s		$I_{GM} = 25 A$	$di_G/dt = 25 A/\mu$ s
E_{on}	Turn-on energy per pulse	2.50 Ws		$C_s = 3 \mu F$	$R_s = 10 \Omega$

Turn-off switching

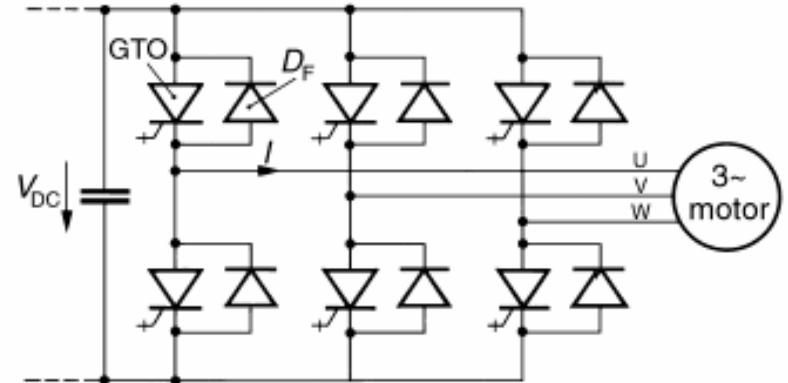
I_{TGQM}	Max controllable turn-off current	3000 A	$V_{DM} = V_{DRM}$	$di_{GQ}/dt = 70 A/\mu$ s
t_s	Storage time	25.0 μ s	$C_s = 3 \mu F$	$L_s \leq 0.2 \mu H$
t_f	Fall time	3.0 μ s		$V_D = 1/2 V_{DRM}$
$t_{off(min)}$	Min. off-time	100 μ s		$V_{DM} = V_{DRM}$
E_{off}	Turn-off energy per pulse	16.0 Ws		$di_{GQ}/dt = 70 A/\mu$ s
I_{GOM}	Peak turn-off gate current	900 A	$I_{TGQ} = I_{TGQM}$	
			$C_s = 3 \mu F$	$R_s = 10 \Omega$
			$L_s \leq 0.2 \mu H$	

GTO

Fig. 13

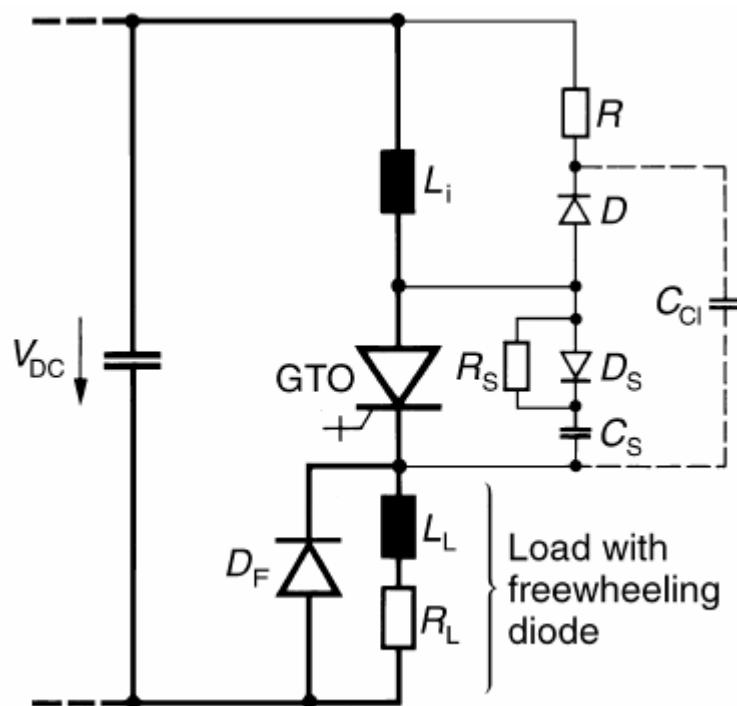
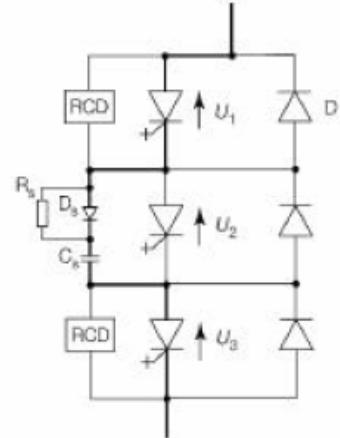
Cathode-side view of various GTO wafers





Basic Circuit of a 3-phase voltage source inverter

Series Connected GTOs



GTO Protection Circuits:

- Turn-on protection (L_i , R , D)
- Turn-off protection (D_s , C_s , R_s , C_{cl})

GTO

(β)

GTO

di/dt

GTO

GTO

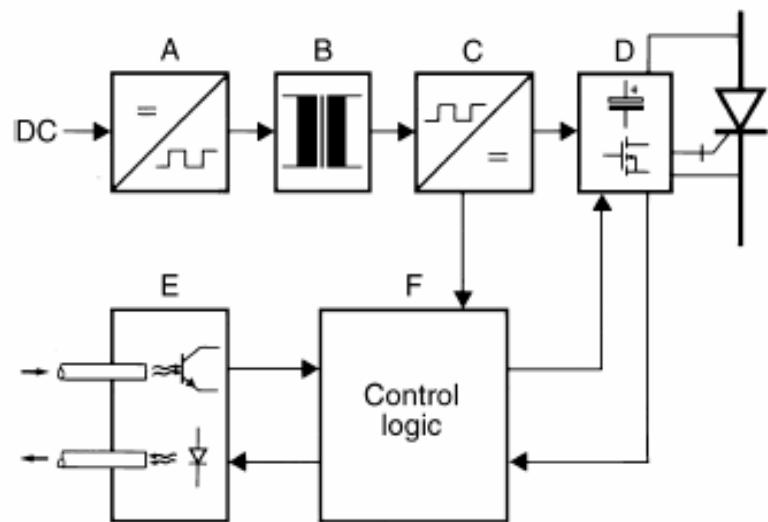


Fig. 5 Block Diagram of Typical GTO Gate Unit

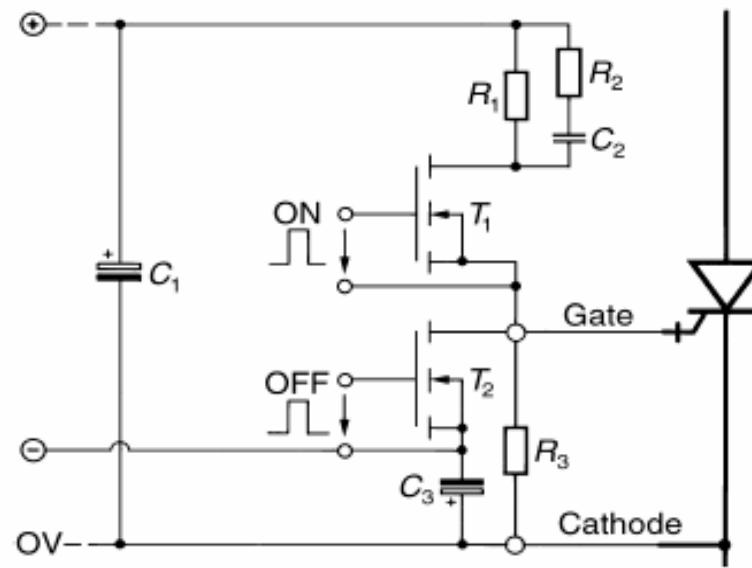
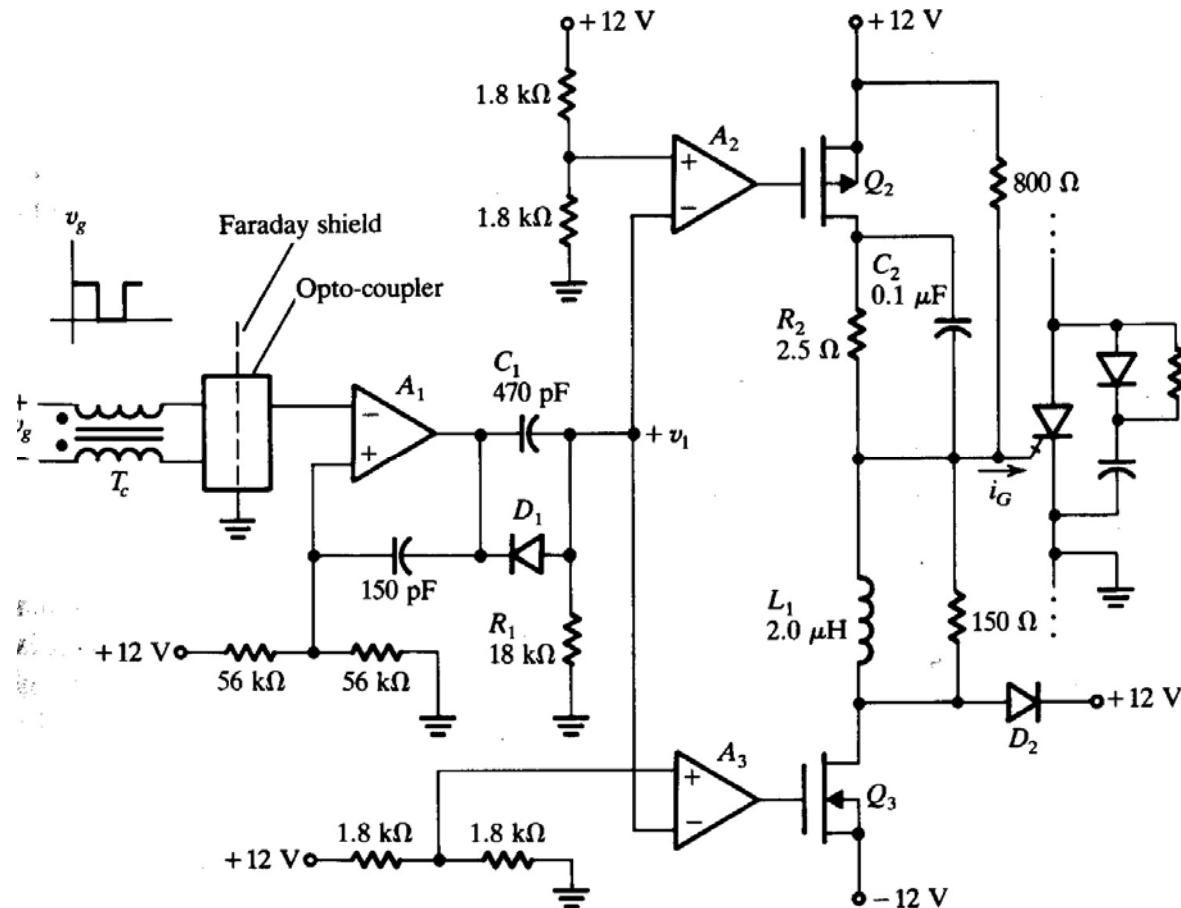


Fig. 6 Possible Circuit for Output Stage D of Fig. 5



Integrated Gate Commutated Thyristor (IGCT)

Key Parameters

V_{DRM}	=	4500 V
I_{TGQM}	=	4000 A
I_{TSM}	=	25 kA
V_{T0}	=	1.2 V
r_T	=	0.37 mΩ
V_{DClink}	=	2800 V

Integrated Gate-Commutated
Thyristor

5SHY 35L4502

PRELIMINARY



Features

- Direct fiber optic control
- Fast response ($t_{don} < 3 \mu s$, $t_{doff} < 6 \mu s$)
- Precise timing ($\Delta t_{doff} < \pm 400 \text{ ns}$)
- Status feedback
- Patented free-floating silicon technology
- Transparent emitter buffer layer technology
- High reliability
- Very high EMI immunity
- Cosmic radiation withstand rating
- Optimized for series connection

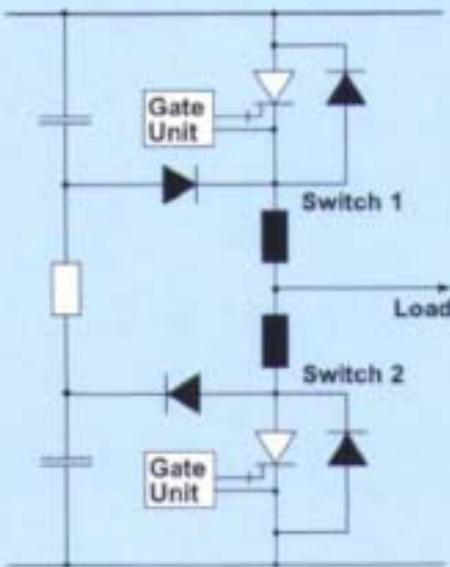
Turn-on switching

di/dt_{crit}	Max. rate of rise of on-state current	1000 A/ μ s	$f = 200$ Hz	$T_j = 115$ °C
			$I_T = 4000$ A	$V_D = 2250$ V
t_{don}	Turn-on delay time	< 2 μ s	$V_D = 2800$ V	$T_j = 115$ °C
t_r	Rise time	≤ 1 μ s	$I_T = 4000$ A	$di/dt = 1000$ A/ μ s
$t_{on(min)}$	Min. on-time	10 μ s	$R_s = 0.80$ Ω	$L_i = 5.0$ μ H
E_{on}	Turn-on energy per pulse	≤ 1 J	$C_{CL} = 6.0$ μ F	$L_{CL} = 0.4$ μ H

Turn-off switching

I_{TGQM1}	Max. controllable turn-off current	4000 A	$V_{DM} \leq V_{DRM}$	$T_j = 115$ °C
			$V_D = 2250$ V	$L_{CL} \leq 0.4$ μ H
I_{TGQM2}	Max. controllable turn-off current	3500 A	$V_{DM} \leq V_{DRM}$	$T_j = 115$ °C
			$V_D = 2800$ V	$L_{CL} \leq 0.4$ μ H
t_{doff}	Turn-off delay time	≤ 6.0 μ s	$V_D = 2800$ V	$V_{DM} \leq V_{DRM}$
t_f	Fall time	≤ 1.0 μ s	$T_j = 115$ °C	$R_s = 0.80$ Ω
$t_{off(min)}$	Min. off-time	10 μ s	$I_{TGQ} = I_{TGQM2}$	$L_i = 5.0$ μ H
E_{off}	Turn-off energy per pulse	≤ 16.0 J	$C_{CL} = 6.0$ μ F	$L_{CL} \leq 0.4$ μ H

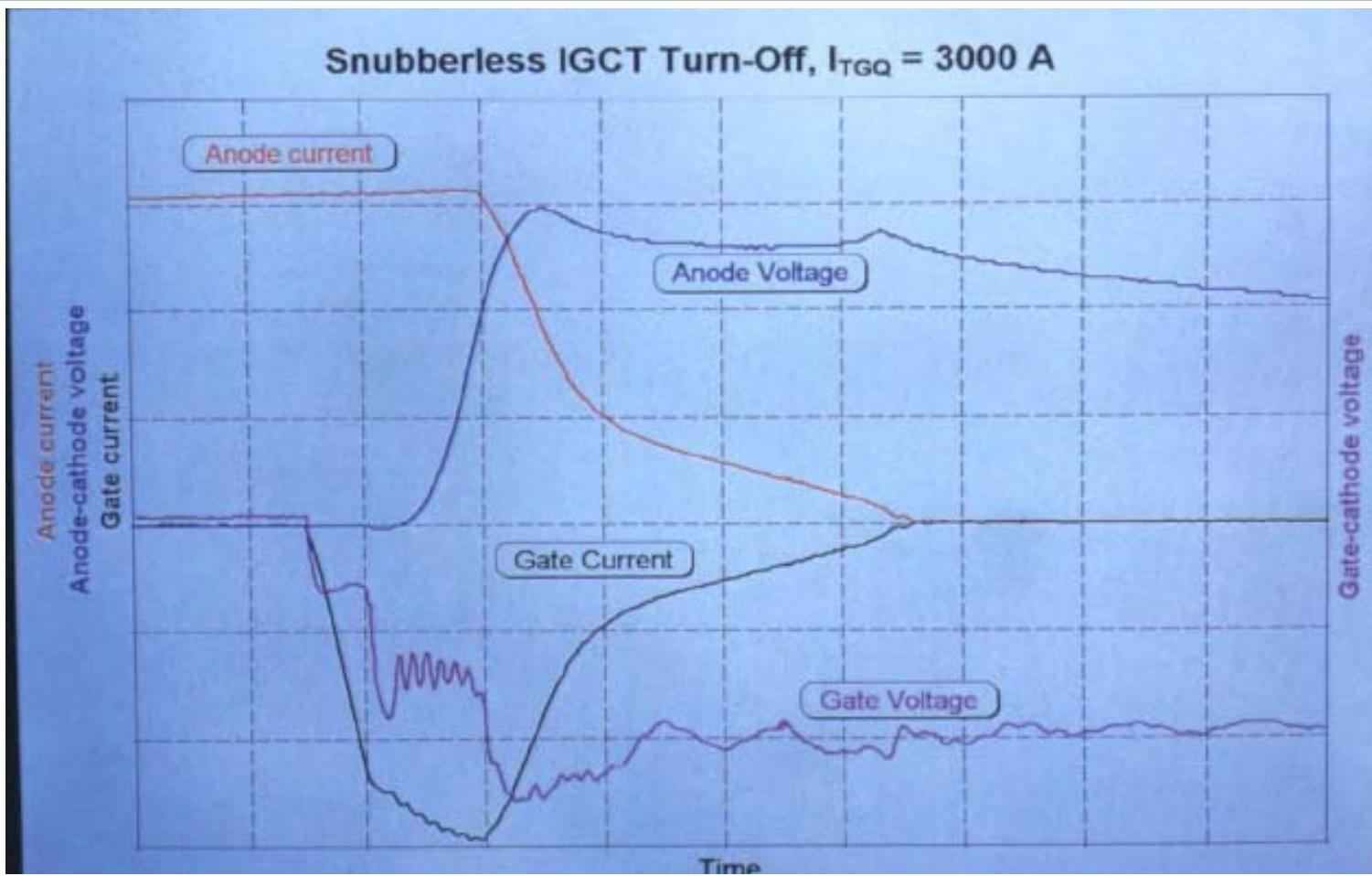
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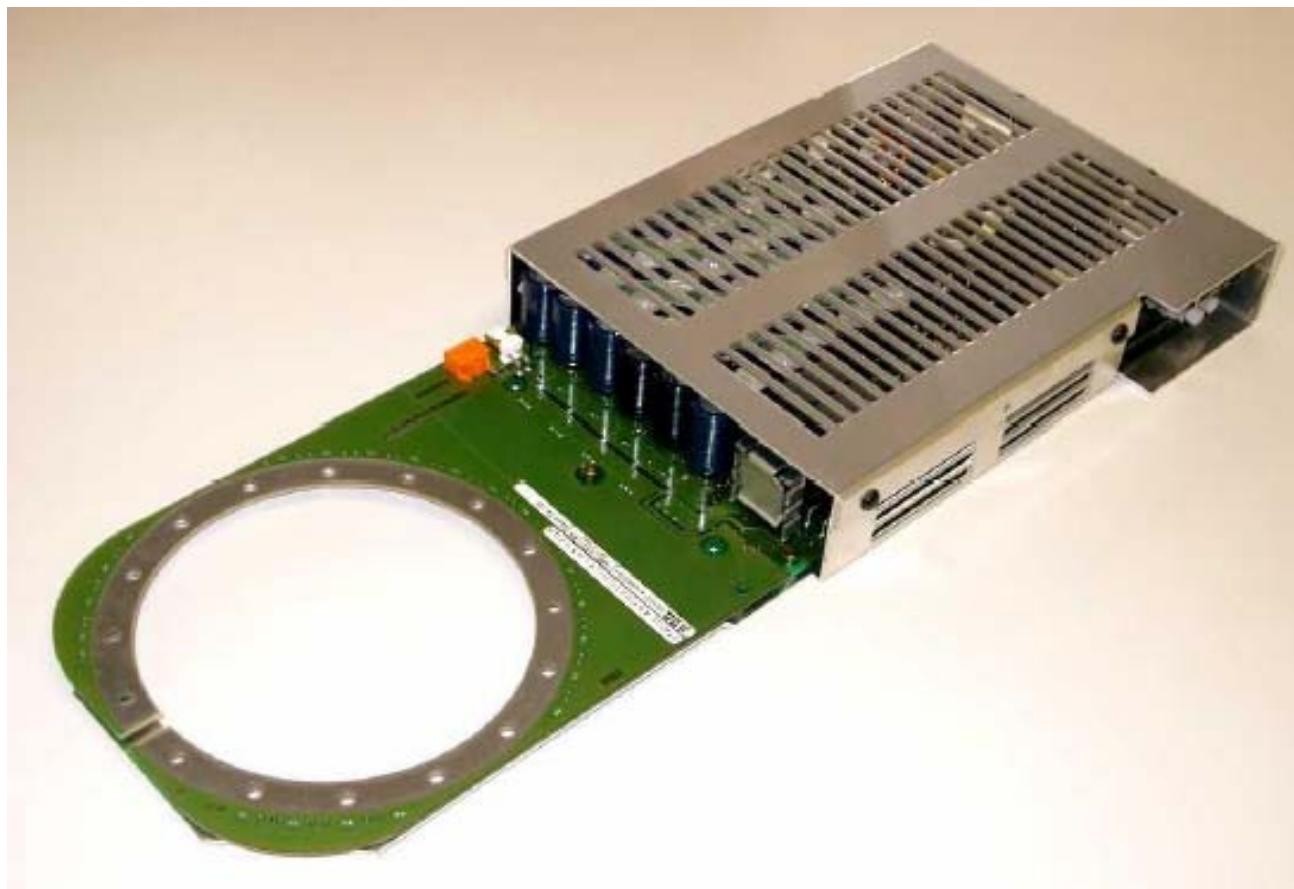
Water cooled
IGCT phase leg



IGCT



IGCT



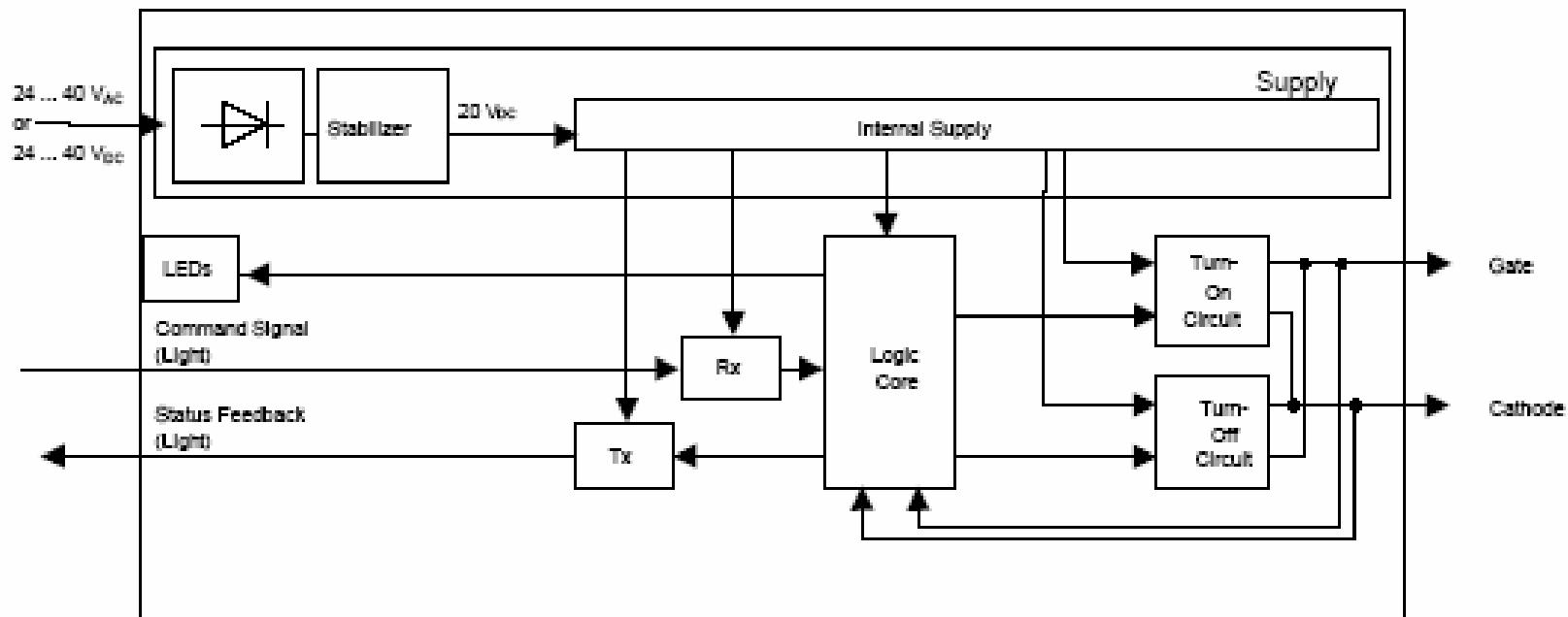
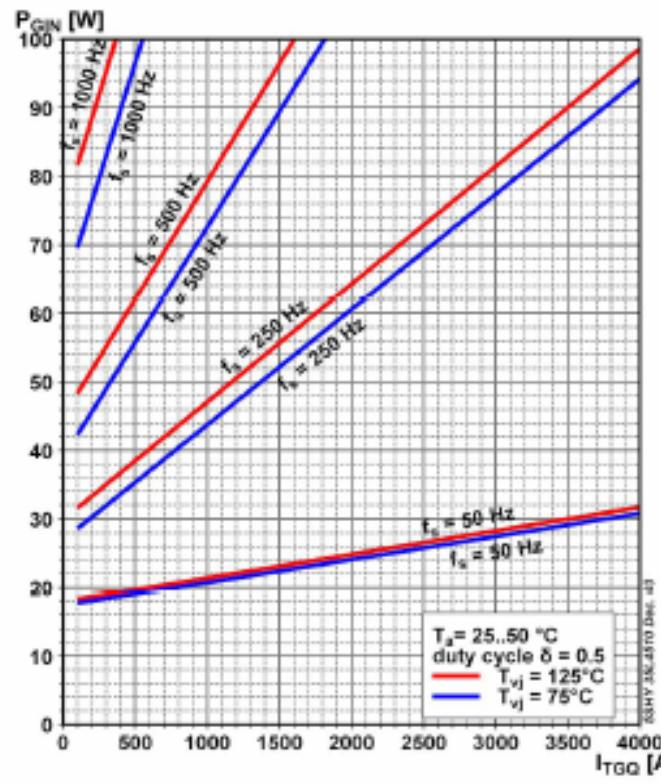


Fig. 1: Block diagram of an IGCT Gate Unit



Maximum Gate Unit input power (dissipated plus transferred) in chopper mode, example